REMARKS

Claims 1-11, 13-41, and 43-57 are pending. Claims 1-5, 9, 11, 17-18, 27, 29-30, 35, 41, and 48-49 are rejected under 35 U.S.C. § 102(e). Claims 1-2, 6-7, 9, 13-16, 36-40, and 54-57 are rejected under 35 U.S.C. § 103(a). Claims 8, 10, 12, 19, 20-26, 28, 31-34, 42-47, and 50-3 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all limitations of the base claim and any intervening claims. Claims 1, 13, 15, 17, 35-36, 39, 41, 43, 54, and 56 are amended. Claims 12 and 42 are cancelled without prejudice.

Claim 12 depends directly from independent claim 1. Claim 1 has been rewritten to include the limitations of claim 12. Claim 12 is cancelled without prejudice. Thus, claim 1 and depending claims 2-11 are patentable under 35 U.S.C. § 102(e).

Claims 17-18, 27, 29-30, and 35 are rejected under 35 U.S.C. § 102(e) as being anticipated by Zyuban et al. (US 2003/0188241). Independent claim 17, as amended, recites "*a first latch coupled to receive a first power supply voltage* for latching a data signal; *a second latch coupled to receive a second power supply voltage less than the first power supply voltage*, said first latch for retaining said data signal while said first latch is inoperative." (emphasis added). This feature of the present invention is described at page 20, line 19 through page 21, line 3. Zyuban et al. fail to disclose such a limitation. Thus, claims 17 and depending claims 18, 27, 29-30, and 35 are patentable under 35 U.S.C. § 102(e).

Claims 41 and 48-49 are rejected under 35 U.S.C. § 102(e) as being anticipated by Zyuban et al. Claim 42 depends directly from claim 41. Claim 41 has been rewritten to include all the limitations of claim 42. Claim 42 is cancelled without prejudice. Thus, claims 41 and 48-49 are patentable under 35 U.S.C. § 102(e).

Claims 1, 2, 6-7, and 11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sani et al. (US 2003/0218231) in view of Coughlin, Jr. et al. (USP 6,493,257). Claim 1, as amended, recites "a first latch *including a plurality of transistors having respective gate oxides* for latching a data signal; a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative; a save device connected between said first and second latches for transferring said data signal from said first latch to said second latch, said save device including a first transistor having a gate *and having a gate oxide that is thicker than said gate oxides of said plurality of transistors*." (emphasis added). These features of the present invention are neither taught nor suggested by a combination of Sani et al. with Coughlin, Jr. et al. Thus, claims 1, 2, 6-7, and 11 are patentable under 35 U.S.C. § 103(a).

Claims 13-16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sani et al. in view of Coughlin, Jr. et al. Independent claims 13 and 15, as amended, recite "a save device connected between said first and second latches for transferring said data signal from said first latch to said second latch, *said save device including a first transistor having a gate and a current path*, said first latch including a node for providing said data signal to said save device, said gate connected to said node, *said save device including a second transistor in series with said current path*." (emphasis added). In the embodiment of Figure 2 of the present invention this is transistor M3. Neither Sani et al. nor Coughlin, Jr. et al. teach or suggest this feature of the present invention. Thus, claims 13-16 are patentable under 35 U.S.C. § 103(a).

Claims 36-40 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Zyuban et al. in view of Sani et al. Independent claims 36 and 39 are amended to recite "*a first latch including a first transistor having a first threshold voltage* for latching a data signal, a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative, and a restore device connected between said first and second latches, *said restore device having an input transistor having a second threshold voltage greater in magnitude than said first threshold voltage* for receiving a restore signal." This feature of the present invention is described at page 6, lines 10-12 with regard to Figure 2. Neither Zyuban et al. nor Sani et al.

teach or suggest this feature of the present invention. Thus, claims 36 and 39 and their respective depending claims 37-38 and 40 are patentable under 35 U.S.C. § 103(a).

Claims 54-57 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Zyuban et al. in view of Sani et al. Independent claims 54 and 56 are amended to recite "*a first latch coupled to receive a first power supply voltage* for latching a data signal, *a second latch coupled to receive a second power supply voltage less than said first power supply voltage* and coupled to said first latch for retaining said data signal while said first latch is inoperative." (emphasis added). This feature of the present invention is described at page 20, line 19 through page 21, line 3. Neither Zyuban et al. nor Sani et al. teach or suggest this feature of the present invention. Thus, claims 54 and 56 and their respective depending claims 55 and 57 are patentable under 35 U.S.C. § 103(a).

In view of the foregoing, applicants respectfully request reconsideration and allowance of claims 1-11, 13-41, and 43-57. If the Examiner finds any issue that is unresolved, please call applicants' attorney by dialing the telephone number printed below.

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